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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Sheet

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of

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<i>Complete if Known</i>	
Application Number	10/627,218
Filing Date	July 25, 2003
First Named Inventor	Yeo, et al.
Art Unit	2831
Examiner Name	Ha
Attorney Docket Number	TSM03-0556

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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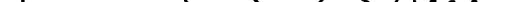
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/627,218
				Filing Date	July 25, 2003
				First Named Inventor	Yeo, et al.
				Art Unit	2831
				Examiner Name	TBD
Sheet	2	of	5	Attorney Docket Number	TSM03-0556

U.S. PATENT DOCUMENTS

Examiner Signature  **Date Considered** 11/3/04

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				First Named Inventor	Yeo, et al.
				Group Art Unit	2831
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0556

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cita. No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
NJH	32	ISMAL, K., et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.			
	33	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.			
	34	GAMIZ, F., et al., "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.			
	35	GAMIZ, F., et al., "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, (July 1, 2002), pp. 288-295.			
	36	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp. 7-14.			
	37	TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, (2002), pp. 96-97.			
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	39	JURCZAK, M., et al., "SON (Silicon on Nothing) – A NEW DEVICE ARCHITECTURE FOR THE ULSI ERA," Symposium on VLSI Technology Digest of Technical Papers, (1999), pp. 29-30.			
	40	MAITI, C.K., et al., "Film Growth and Material Parameters," Application of Silicon-Germanium Heterostructure, Institute of Physics Publishing, Ch. 2 (2001) pp. 32-42.			
	41	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp. 939-941.			
	42	OOTSUKE, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meeting, (2000), pp. 575-578.			
↓	43	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.			
NJH	44	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," Journal of Crystal Growth, Vol. 29, (1975), pp. 273-280.			
Examiner Signature	<i>[Signature]</i>			Date Considered	11/20/03

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NH	45	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
	46	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.	
	47	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1 (Jan./Feb. 1975), pp. 126-133.	
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	49	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
	50	SHIMIZU, A., et al., "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
	51	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
	52	YANG, F.L., et al., "25 nm CMOS Omega FETs," IEDM 2002, pp. 255-258.	
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	54	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um ² SRAM Cell," IEDM, pp. 61-64.	
	55	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.	
	56	BLAAUW, D., et al., "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.	
NH	57	"Future Gate Stack," International Sematech, 2001 Annual Report.	

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